REMARKS/ARGUMENTS

After entry of this amendment, claims 20 and 23, 25-28 and 30-35 will be pending in this application. Claims 1, 3, 10-19, 24, and 29 have been cancelled without prejudice. Claims 31-35 have been added. Claims 23, 25, 26, 27, and 30 have been amended. Support for the new and amended claims can be found in the specification, no new matter has been added. Claim 20 has been indicated as being allowable if rewritten as an independent claim. Accordingly, claim 20 has been made independent.

Claims 1, 3, 10-18, 25, and 26 stand rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi et al. "Architecture and Implementation of a Highly Parallel Single-Chip Video DSP" (Yamauchi). Claim 19 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi.

Reconsideration of these rejections and allowance of the pending claims in light of these amendments and remarks is respectfully requested.

Claim 23

Claim 23 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi. But Yamauchi does not teach each and every element of this claim. For example, claim 10, as amended, recites "a shared operand unit coupled to provide a shared operand to the first MAC unit, the second MAC unit, the third MAC unit, and the fourth MAC unit." Yamauchi does not provide this feature.

The pending office action cites IN1 of Figure 2 of Yamauchi as being a shared operand unit. But this structure only couples to two MAC units. Accordingly, Yamauchi does not provide a shared operand unit coupled to provide a shared operand to the first MAC unit, the second MAC unit, the third MAC unit, and the fourth MAC unit as required by the claim.

For at least this reason, claim 23 should be allowed.

Claim 25

Claim 25 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi. But Yamauchi does not teach each and every element of this claim. For example,

claim 25, as amended, recites "a first communication port coupled to the first embedded processor and the first array processor, for communicating with a second array processor and a second embedded processor." Yamauchi does not provide this feature.

By providing a communication port as recited, embodiments of the present invention increase the parallel processing capabilities. Yamauchi does not provide this benefit.

For at least this reason, claim 25 should be allowed.

Other claims

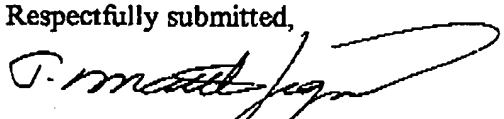
Claims 27 and 31 should be allowed for similar reasons as above. The remaining pending claims depend on these claims, and should be allowed for the same reasons, and the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



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